	Type	L #	Hits	Search Text	DBs	Time Stamp
1	IS&R	L1	10	(("4577215") or ("5266519") or ("4357685") or ("5287536") or ("5414297") or ("5131444") or ("4597000") or ("5187583") or ("5216269") or ("5634445")).PN.	USPAT; US-PGPUB	2002/07/12 09:30
2	IS&R	L2	39	(("5479992") or ("5978272") or ("6046186") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("5687115") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("4903097") or	USPAT; US-PGPUB	2002/07/12 09:30
3	BRS	L6	12	5 not (2 or 1)	USPAT; US-PGPUB	2002/07/12 09:43
4	IS&R	L5	12	(("[illegible]2") or ("5295344") or ("5415541") or ("5343063") or ("[illegible]") or ("5313421") or ("5712180") or ("[illegible]") or ("[illegible]") or ("[illegible]") or ("5043940") or ("5172338") or ("5651881")).PN.	USPAT; US-PGPUB	2002/07/12 09:43

	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Inventor
1	US 5216269 A	[illegible]0601	13	Electrically-programmable semiconductor memories with buried injector region	257/319	257/320; 365/185.3; 365/185.31	Middelhoek, Jan et al.
2	US 4577215 A	19860318	8	Dual word line, electrically alterable, nonvolatile floating gate memory device	257/319	365/185.14; 365/185.18	Stewart, Roger G. et al.
3	US 6240015 B1	[illegible]0529	14	Method for reading 2-bit ETOX cells using gate induced drain leakage current	365/185.14	365/185.01; 365/185.26	Chi, Min-hwa et al.
4	US [illegible]13100 B1	[illegible]0403	22	Nonvolatile memory cell and method for programming and/or verifying the same	365/185.14	365/185.03; 365/185.2; 365/185.22; 365/185.26	Choi, Woong Lim
5	US 6034892 A	20000307	22	Nonvolatile memory cell and method for programming and/or verifying the same	365/185.14	365/185.01; 365/185.28	Choi, Woong Lim
6	US 5751635 A	19980512	79	Read circuits for analog memory cells	365/185.19	327/93; 327/94; 365/185.03; 365/185.2; 365/185.21	Wong, Sau C. et al.
7	US 5387534 A	19950207	11	Method of forming an array of non-volatile sonos memory cells and array of non-violatile sonos memory cells	438/287	438/296; 438/302	Prall, Kirk
8	US 5218569 A	19930608	23	Electrically alterable non volatile memory with n bits per memory cell	365/185.21	365/185.19; 365/185.2; 365/185.22; 365/185.29; 365/186; 365/45	Banks, Gerald J.

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	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Inventor
1	US 6272042 B1	20010424	37	Multi-state memory	365/185.03	365/185.2; 365/185.21; 365/185.22	Guterman, Daniel C. et al.
2	US 5851881 A	19981222	18	Method of making monos flash memory for multi-level logic	438/261	438/264; 438/296	Lin, Ruei-Ling et al.
3	US 5313421 A	19940517	28	EEPROM with split gate source side injection	365/185.17	365/185.01; 365/185.18; 365/185.14; 365/185.15; 365/185.22; 365/185.2; 365/185.31	Guterman, Daniel C. et al.
4	US 5172338 A	19921215	44	Multi-state EEprom read and write circuits and techniques	365/185.03	365/184; 365/185.33; 365/189.07; 365/195; 365/201	Mehrotra, Sanjay et al.
5	US 5095344 A	19920310	49	Highly compact EPROM and flash EEPROM devices	257/328	257/327; 257/488; 365/185.03; 365/185.09; 365/185.18; 365/185.2; 365/185.22; 365/185.27; 365/185.3; 365/185.31; 365/185.33	Harari, Eliyahou
6	US 5043940 A	19910827	14	Flash EEPROM memory systems having multistate storage cells	365/185.03	365/185.09; 365/185.11; 365/185.19; 365/185.2; 365/185.22; 365/185.25; 365/185.3; 365/185.33; 365/218	Harari, Eliyahou

	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Inventor
1	US 5838041 A	19981117	15	Nonvolatile semiconductor memory device having memory cell transistor pr[illegible]d with offset region acting as a charge carrier injecting region	257/324	257/326	Sakagami, Eiji et al.
2	[illegible] 5654568 A	19970805	24	Semiconductor device including nonvolatile memories	257/324	257/295; 257/314; 257/326	Nakao, Hironobu
3	US 4481527 A	19841106	8	High density MNOS transistor with ion implant into nitride layer adjacent gate electrode	257/325	257/326; 257/394; 257/390; 365/178; 365/184	Chen, Yung J. et al.
4	[illegible] 4542399 A	19850917	9	Electrically erasable programmable MNOS read only memory	365/104	257/326; 365/184	Kuo, Chang Kiang
5	US 4057820 A	19771108	5	Dual gate MNOS transistor	257/326	148/DIG.156	Gallagher, Robert C.
6	US 3925804 A	19751209	17	Structure of and the method of processing a semiconductor matrix or MNOS memory elements	257/326	320/106	Cricchi, James Ronald et al.

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